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1. INTRODUCTION

As the nation's primary weather radar system for the next 20-30 years, the WSR-88D network must continue to evolve to meet increasing users' demand for performance and capability. The expected life of this system is much longer than the technology utilized within. Therefore evolution is also necessary to keep life cycle logistic and maintenance efforts manageable.

Many parallel efforts are currently underway to enhance existing capabilities and implement new features. These efforts are primarily in the Radar Product Generator (RPG) and the Principal User Processor (PUP) functional areas. Many proposed features such as the polarimetric capability require significant modification and redesign of the signal acquisition and processing subsystem in the Radar Data Acquisition (RDA) functional area.

This paper presents preliminary work undertaken by the National Severe Storms Laboratory (NSSL) to provide significant improvements in the RDA area. Although, the ultimate goal is to provide polarimetric capability for the WSR-88D, achievement of this goal depends entirely on an intermediate yet equally important task, replacement of the existing RDA status and control computer (RDASC), the hardwired signal processor (HSP), and the programmable signal processor (PSP) with modern more powerful equipment. The paper will focus on the architecture and design of the prototype host computer and signal processing system currently under development at the NSSL.

2. SYSTEM COMPONENTS

The RDA essentially consists of an antenna, it's pedestal, a transmitter, a receiver, and associated data acquisition and control equipment. The transmitter is a coherent pulsed S-band design using a klystron tube. The antenna is a 28 ft. diameter center-fed parabolic reflector with a 0.95 degree beamwidth. Servo amplifiers for the antenna are controlled by a digital control unit (DCU) which provides position information to, and receives commands from the host computer on regular intervals.

The signal acquisition components consist of a receiver

feeding digital samples of returned echoes to a digital signal processor. The receiver uses fast automatic gain control (AGC) and provides 12-bit in-phase (I), 12-bit quadrature (Q) and 6-bit AGC attenuator values at 250 meter range intervals.

Real-time monitoring and control is provided by a host computer executing users' commands issued either locally or from a remote location. The WSR-88D is equipped with a data acquisition unit (DAU) to collect and monitor status of all the components in the RDA including power supply voltages, environmental conditions, and the state of safety interlocks. This information is transmitted to the host computer in regular intervals to determine the state of the system.

Figure 1 illustrates the proposed functional configuration of the RDA. Some support functions are implied in this diagram and not directly shown. The second receiver shown in this diagram is for simultaneous reception of horizontal and vertical components when polarimetric capability is fully implemented. The shaded area highlights the components affected by the first phase of this project and is the primary focus of this paper.

3. RDA ARCHITECTURE

The long expected life of the WSR-88D coupled with increasing demands for new features and improved performance mandate a modular and scalable architecture. Such an architecture will readily accommodate gradual and systematic technology insertion to implement new features and reduce the impact of obsolescence. Open system standards were developed to allow interoperability between functional modules and reuse of valuable components. Although highly desirable, open system concepts can only be

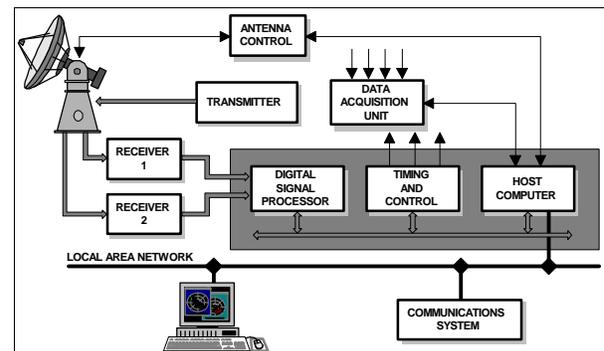


Figure 1: Simplified Block Diagram of the RDA

partially applied in this case. There are many specialized and custom components in the RDA for which no standards exist.

Based on these considerations and constraints, a multiprocessor architecture has been designed for the RDA signal processing and control (RDASPC) platform with primary emphasis on a design which is highly modular and expandable. Open system concepts and commercial-off-the-shelf (COTS) equipment have been utilized to the maximum possible extent. Based on this design a development environment has been established and a prototype is currently under construction. Figure 2 shows a simplified block diagram of the proposed platform.

4. PLATFORM CHARACTERISTICS

The proposed RDA computing platform is based on ANSI standard VME-64 chassis and equipment. Popularity and widespread support of the VME bus render it the prime candidate for this application. VME is currently the most popular common bus architecture and will likely remain so for the foreseeable future.

In this design a real-time host processor controls various functional elements interconnected through a standard VME-bus chassis. The host computer manages and performs task initiation, process scheduling, resource management, status monitoring and control, antenna operations, and data transfer. Using VME bus, a large number of choices exist for the host computer. Many manufacturers offer highly integrated yet inexpensive single board computers suitable for this application. For the prototype, a Motorola™ single board computer equipped with a 50MHz MC68060™ processor was chosen. This board features up to 128 megabytes of memory, 4 serial ports, a parallel port, SCSI port, and an Ethernet interface. A PowerPC™ solution is also under development.

Antenna control and DAU connections are implemented with standard asynchronous serial ports on the host computer.

The Ethernet interface allows local area network (LAN) connectivity. In Figure 1, for example, a development workstation is shown connected to the real-time host through the LAN. The workstation can also be used for interactive

maintenance and diagnostic sessions. Full or partial open system RPG (ORPG) functionality can also be locally provided using the workstation and appropriate software modules. Indeed, an ORPG can be seamlessly integrated within this architecture by using common networking protocols.

A synchronization and timing module (synchronizer) produces all required timing pulses for the transmitter and receivers including built-in test and calibration sequences.

The signal processing subsystem consisting of an array of processing elements connected through its own high-speed interconnect is also integrated on the VME-bus. Data from one or more receivers are provided directly to the DSP subsystem. These data streams are not provided on the VME-bus since they could easily consume available VME-bus bandwidth. The programmable DSP array performs prescaling, clutter filtering and all base data estimation algorithms.

The dual-port memory allows simultaneous access to control structures and real-time data by the host computer and the DSP array. Dual-port memory devices can efficiently provide process synchronization and interprocess communication in a multiprocessor environment. The memory module used in the RDASPC prototype is a 256 megabyte DRAM module manufactured by Micro Memory Inc. This module can be expanded to 512 megabytes.

Real-time characteristics of RDA control functions require efficient and deterministic behavior from the controlling software. Therefore a real-time operating system is mandatory for the RDA platform. For the development environment and the prototype the VxWorks™ operating system was chosen. VxWorks is a scalable operating system which supports a large variety of target processors and has extensive multiplatform development tools. It conforms to the POSIX standard.

5. DIGITAL SIGNAL PROCESSOR SUBSYSTEM

Bulk of the numerical processing in the RDA falls in the DSP domain. Radar signal estimation algorithms operate on a relatively large number of range bins. Individual routines can often be described by the single instruction multiple data stream (SIMD) model. Yet different procedures are

performed on the data set in prescribed sequences depending on the acquisition mode and atmospheric conditions. This can effectively be described by a pipeline model. The DSP subsystem should therefore be flexible and easily reconfigurable. It should provide relatively large number of processors and an efficient mechanism to transfer data from one processing stage to another to exploit inherent parallelism in radar signal processing applications.

The DSP subsystem chosen for the prototype is

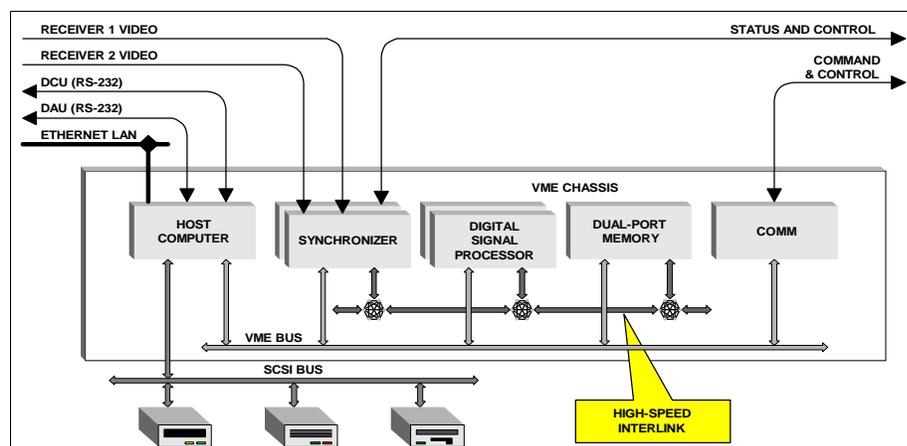


Figure 2: Simplified Block Diagram of the RDASPC

based on the Mercury Computer Systems' RACE® architecture, RACEway. RACEway is a switched interconnect fabric build with crossbar switches. As opposed to conventional buses which can only accommodate one transaction at a time, the RACE interconnect can accommodate multiple transactions simultaneously. The fundamental building block of the RACEway is a 6-port crossbar switch depicted in Figure 3. Each port is 32-bits wide and as long as a path between two ports does not cross another path it can sustain a transaction at peak rate of 160 megabytes per second. RACEway has been adopted as the RACEway Interlink standard (ANSI/VITA 5-1994).

The RACEway can be extended using interlink modules connected to the VME P2 connector. This will yield virtually unlimited scalability. Using this architecture, one can connect relatively large number of compute nodes (CN) by a very high-bandwidth, low-latency, circuit-switched crossbar network. A typical arrangement currently implemented as one of the development platforms is shown in figure 4. Terminal nodes may be comprised of computing elements, stand-alone memory, standard bus interfaces, or dedicated I/O devices.

Compute nodes used in this application are also manufactured by Mercury Computer Systems, Inc. They utilize the Analog Devices' ADSP-21060 Super Harvard Architecture Computer (SHARC™) chips. SHARC is the first of a modern family of high-performance highly integrated DSP devices recently introduced. Each processor has 4 Mbits of high-speed static RAM and can execute up to 120 MFLOPS or a 512 point real FFT in 136 microseconds. Each compute node is equipped with 3 SHARCs, 16 megabytes of memory, and an application specific integrated circuit (ASIC)

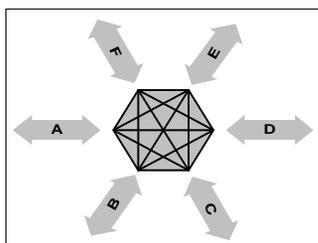


Figure 3: RACEway Crossbar

which contains all support and interface circuits including a direct memory access (DMA) controller. Figure 5 illustrates a simplified block diagram of the SHARC compute node.

In the configuration shown in Figure 4, two 6U VME modules are interconnected using an 8-slot interlink module. One VME module contains a high-speed input interface, RIN-T™, and two compute nodes, and the other module contains four compute nodes for a total of 18 processors capable of 2.16 GFLOPS peak. Test routines have been developed for simulation and benchmarking of WSR-88D algorithms for clutter filtering and base data derivation on 600 range bins using 64 pulses. These procedures require only four SHARCs.

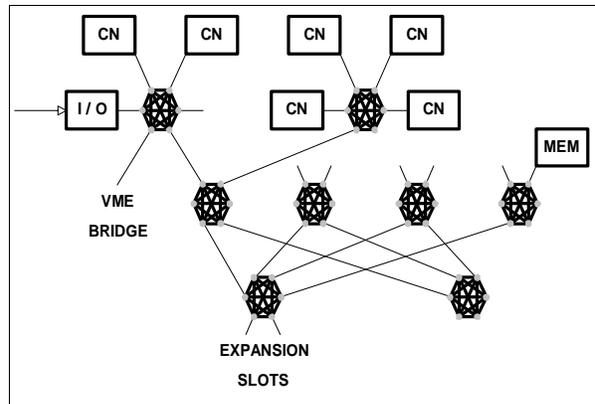


Figure 4: A Typical Multiprocessor Configuration

6. RADAR TIMING AND SYNCHRONIZATION

The WSR-88D is a very complex real-time control and acquisition system. The transmitter and the receiver require precise timing pulses to generate the transmitted pulse and sample the returned echoes. Sophisticated built-in test and calibration circuitry is exercised every volume scan to verify proper operation and accuracy of parameters extracted by the operating software. In fact, approximately 80 signals must be either accurately monitored or precisely generated during every volume scan. Another 60 or more signals will be added when polarimetric capability is implemented.

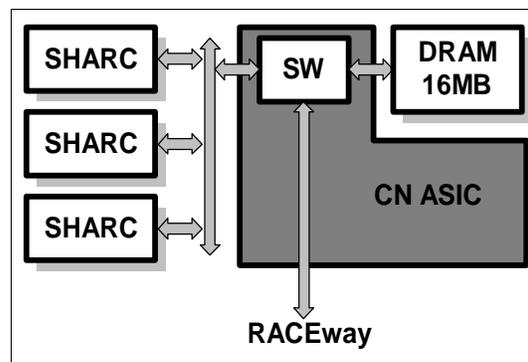


Figure 5: SHARC Compute Node

In the prototype RDA timing functions will be implemented using a custom synchronizer module. This module is based on a modern design featuring much improved flexibility yet significantly lower number of components. A simplified block diagram of the new synchronizer is shown in Figure 6. This design is based on an integrated programmable sequencer engine which is in fact part of a powerful fixed-point DSP, Analog Devices' ADSP-2181. Using a master clock signal derived from the coherent oscillator, the sequencer operates at approximately 20 MIPS providing timing resolution of 52 nanoseconds. The sequencer receives commands from the host computer and generates timing signals according to an appropriate set of command primitives encoded in high-speed flash memory. All logic functions within the synchronizer are implemented using erasable programmable logic devices, thus providing ultimate flexibility in both form and function.

The receiver interfaces are also implemented using high-speed reprogrammable logic devices. These interfaces convert incoming digital video signals from the receiver(s) to parallel data, synchronize each sample with corresponding AGC attenuator value, and convert the result to an IEEE 32-bit floating-point number and send the final result to the DSP array. Once initiated, the entire conversion and transfer process takes place without further intervention by the sequencer.

A prototype synchronizer has been fabricated and is currently undergoing initial tests.

7. ACKNOWLEDGMENT

The WSR-88D is jointly maintained and operated by the National Weather Service (NWS), a component of the National Oceanic and Atmospheric Administration (NOAA), in the Department of Commerce (DOC), the Air Force's Air Weather Service (AWS), in the Department of Defense (DOD), and the Federal Aviation Administration (FAA) in the Department of Transportation (DOT). The primary support organization established by the three agencies is the WSR-88D Operational Support Facility (OSF). The authors also wish to acknowledge the NWS Office of Systems Development (OSD) for project management and support for the WSR-88D evolution. The NSSL along with other ERL laboratories provide technical leadership and guidance in further understanding and utilization of the WSR-88D

system.

The authors also wish to acknowledge Dr. Dusan Zrnica for his leadership and Mr. Mike Schmidt and Mr. Richard Wahkinney for their support in maintaining the radar and fabricating the prototype equipment.

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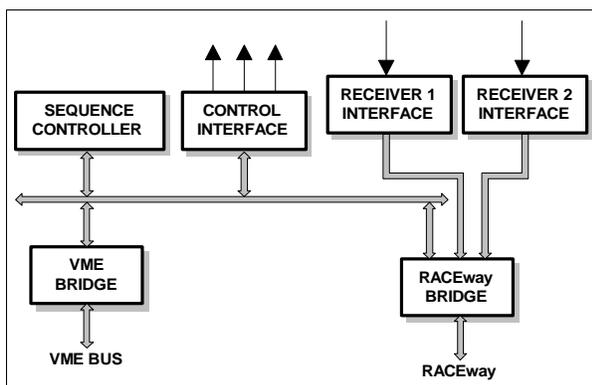


Figure 6: RDA Synchronizer